UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Magerlein et al.

Serial No.:

10/052,619

For:

TEMPORARY DEVICE ATTACH STRUCTURE FOR TEST AND

BURN IN OF MICROJOINT INTERCONNECTS AND METHOD RECEIVED

TC 1700

FOR FABRICATING THE SAME

Filed:

January 18, 2002

Examiner:

Not Yet Assigned

Art Unit:

Not yet assigned

fee set forth in 37 C.F.R. §1.17(p);

Attorney Docket:

YOR920010249US1

COPY OF PAPERS ORIGINALLY FILED

Commissioner for Patents Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

In accordance with applicant's duty of disclosure under 37 C.F.R. §1.56, please find attached hereto form PTO-1449 listing information which may be material to the patentability of this application, filed concurrently herewith. This Information Disclosure Statement is being filed:

<u>XXX</u>	Within three (3) months of the filing date of the national application;
	Within three (3) months of the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application;
	Before the mailing date of a first Office Action on the merits;
	After the filing date or date of first Office Action, but before the mailing date of a final action under 37 C.F.R. §1.113, provided that this occurs prior to the issuance of a Notice of Allowance and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e) or the fee set forth in 37 C.F.R. §1.17(p);
	After the filing date or date of first Office Action, but before the mailing date of a Notice of Allowance under 37 C.F.R. §1.311, provided that this occurs prior to the final action and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e) or the

After the mailing date of a final action under 37 C.F.R. §1.113, provided that this occurs prior to the issuance of a Notice of Allowance and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e), a petition requesting consideration of the I.D.S., and the petition fee set forth in 37 C.F.R. §1.17(i)(1); and

After the mailing date of a Notice of Allowance und r 37 C.F.R. §1.311, provided that this occurs prior to the issuance of a final action and provided that this I.D.S. is accompanied by either a certification as specified in 37 C.F.R. §1.97(e), a petition requesting consideration of the I.D.S., and the petition fee set forth in 37 C.F.R. §1.17(I)(1).

Enclosed are copies of U.S. Patent Nos.

6,339,024, 6,344,125; and 6,368,484.

Also enclosed is copy of specification of pending U.S. patent application: Richard Volant, Kevin Petrarca, Peter Locke, James A. Tornello and Donald F. Canapri, Tittle: "REPLATED METAL STRUCTURES FOR SEMICONDUCTOR DEVICES", U.S. Patent Application Serial No. 09/567,469, filed May 9, 2000.

It should be understood that attention has been called to the references that have been deemed to be pertinent to the claimed present invention. In concluding what was pertinent, the criteria employed was considered most appropriate in light of the invention shown in the present application. However, the Examiner or others may deem some other criteria to be just as appropriate or more appropriate. Therefore, the Examiner is respectfully urged to review the listed references and to make the usual careful independent search for other prior art that may be pertinent.

Respectfully submitted,

April 12, 2002

Date

APR 26 2002 Reg. No. 31,019
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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

Docket Number (Optional)	Application Number
YOR9200010249US1	10/052,619
Applicant	

Magerlein et al.

Filing Date

Group Art Unit

(Us several sheets if necessary)

January 18, 2002

Not yet assigned

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING I	
	6,339,024	1/15/02	Petrarca et al.	438	686		
	6,344,125	2/5/02	Locke et al.	205	118		
	6,368,484	4/9/02	Volant et al.	205	220		
						-	
		F01	PEION DATENT DOCUME	NITC			
		FUF	REIGN PATENT DOCUME	1 1 1 1 1 1			
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	lation NO

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)

Richard Volant, Kevin Petrarca, Peter Locke, James A. Tornello and Donald F. Canaperi, Tittle: "Replated Metal Structures for Semiconductor Devices", U.S. Patent application Serial No. 09/657,469, filed on May 9, 2000.

RECEIVED DATE CONSIDERED

EXAMINER

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through